Doe Hyun Yoon – Research Staff Member at IBM Thomas J. Watson research center

CONTACT INFORMATION

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RESEARCH INTERESTS

Broad range of computer architecture, including hardware, software, and co-design. Past research includes memory systems, high-performance computing, system reliability, energy efficiency, audio and video codec, and sorting algorithms.

EDUCATION

The University of Texas at Austin, Austin, Texas, USA
Ph.D. in electrical and computer engineering [MAY 2011]
- Computer engineering (CE) track in electrical and computer engineering
- Dissertation: Flexible and Efficient Reliability in Memory Systems
- Advisor: professor Mattan Erez

Stanford University, Stanford, California, USA
Master of Science in Electrical Engineering [JUN 2007]

Yonsei University, Seoul, Korea
Master of Science in Electrical and Computer Engineering [FEB 2000]
- Dissertation: A Study on an Efficient Test for SRAM using Dynamic Power Supply Current
- Advisor: professor Sungho Kang

Bachelor of Science in Electrical Engineering [FEB 1998]

WORK AND RESEARCH EXPERIENCE

IBM Thomas J. Watson research center, Yorktown Heights, New York, USA
Research staff member [JUN 2013 – PRESENT]
- **Manager:** Fabrizio Petrini
- Research on high-performance computing
- Developing an accurate, portable performance model for data-intensive algorithms such as sorting.

Intelligent Infrastructure Lab., HP Labs, Palo Alto, California, USA
Post doctoral researcher [JUL 2011 – APR 2013]
- **Managers:** Partha Ranganatha, Robert Schreiber, and Dejan Milojicic
- Energy proportional server memory systems using mobile memory.
- Multiversioned nonvolatile memory systems for failure atomicity, consistency, and durability support.
- 3-level cell phase change memory to tolerate resistance drift.

Research associate (Summer intern) [MAY 2010 – AUG 2010]
- **Mentors:** Naveen Muralimanohar, Jichuan Chang, Partha Ranganathan, and Norm Jouppi
- Fine-grained data remapping for tolerating wear-out failures in nonvolatile memory.

LPH research group, The University of Texas at Austin, Austin, Texas, USA
Research assistant [JAN 2008 – MAY 2011]
- **Advisor:** Mattan Erez
- Efficient and flexible reliability in memory systems: two-tiered protection, virtualized ECC, and the dynamic granularity memory system.
- Participated in the initial development of system-level reliability, *Containment Domains*.

Design verification team, MIPS Technology, Mountain View, California, USA
Engineering intern [JUN 2006 – SEP 2006]
- **Manager:** Chinh Tran
- Developed a coverage analysis tool for on-chip bus transactions, analyzing L2 cache transaction requests.

Digital Media research lab., LG Electronics, Seoul, Korea
Senior research engineer [MAR 2004 – SEP 2005]
- Research in scalable video coding (SVC), including standard activity in the MPEG/JVT meetings.
- Worked on real-time OS, managing real-time tasks in TI OMAP chip for LGE's 3G cell phone products.

Junior research engineer [Jan 2000 – Feb 2004]
- Developed MP3/H.263/H.263+/MPEG-4 simple profile on TI DSPs, including algorithms, floating point to fixed point conversion, C and assembly level optimization, DMA-based frame buffer management. error resilience / concealment, QoS improvement, and Inter-Operability Testing.

Computer systems lab., Yonsei University, Seoul, Korea
Research Assistant [Jan 1998 – Dec 1999]
- **Advisor:** Sungho Kang
- Studied VLSI testing: SRAM current testing and test pattern compaction.

Teaching Experience

Teaching assistant
EE360N computer architecture, The University of Texas at Austin
- Fall 2008 (class by professor Derek Chiou) and Spring 2008 (class by professor Mattan Erez)

EE265 signal processing lab., Stanford University
- Spring 2007 (class by professor Teresa Meng)
- Fall 2006 and Winter 2007, class preparation: lab guidelines and solutions with Caleb Kemere and professor Teresa Meng

Publications: Conferences, Journals, and Magazines

Jishen Zhao, Sheng Li, Doe Hyun Yoon, Yuan Xie, and Norman P. Jouppi
"**Kiln: Closing the Performance Gap Between Systems With and Without Persistence Support**,"
(to appear) in *Proc. the 46th Ann. IEEE/ACM Int'l Symp. Microarchitecture (MICRO)*, Dec. 2013.

Doe Hyun Yoon, Jichuan Chang, Robert S. Schreiber, and Norman P. Jouppi
"**Practical Nonvolatile Multilevel-Cell Phase Change Memory**,"
(to appear) in *Proc. the Int'l. Conf. High Performance Computing, Networking, Storage and Analysis (SC)*, Nov. 2013.

Doe Hyun Yoon, Min Kyu Jeong, Michael Sullivan, and Mattan Erez
"**Towards Proportional Memory Systems**,"
in *Intel® Technology Journal*, Vol. 17, Issue 1, pp. 118-139, 2013.

Jinsuk Chung, Ikhwan Lee, Michael Sullivan, Jee Ho Ryoo, Dongwan Kim, Doe Hyun Yoon, Larry Kaplan, and Mattan Erez
"**Containment Domains: A Scalable, Efficient, and Flexible Resiliency Scheme for Exascale Systems**,"
in *Proc. the Int'l. Conf. High Performance Computing, Networking, Storage and Analysis (SC)*, Nov. 2012.

Sheng Li, Doe Hyun Yoon, Ke Chen, Jishen Zhao, Jung Ho Ahn, Jay Brockman, Yuan Xie, and Norman P. Jouppi
"**MAGE: Adaptive Granularity and ECC for Resilient and Power Efficient Memory Systems**,"
in *Proc. the Int'l. Conf. High Performance Computing, Networking, Storage and Analysis (SC)*, Nov. 2012.

Doe Hyun Yoon, Jichuan Chang, Naveen Muralimanohar, and Parthasarathy Ranganathan,
"**BOOM: Enabling Mobile Memory Based Low-Power Server DIMMs**,"
in *Proc. the 39th Ann. Int'l Symp. Computer Architecture (ISCA)*, Jun. 2012.

Doe Hyun Yoon, Mike Sullivan, Min Kyu Jeong, and Mattan Erez,
"**The Dynamic Granularity Memory System**,"
in *Proc. the 39th Ann. Int'l Symp. Computer Architecture (ISCA)*, Jun. 2012.

Doe Hyun Yoon, Tobin Gozalez, Parthasarathy Ranganathan, and Robert S. Schreiber,
"**Exploring Latency-Power Tradeoffs in Deep Nonvolatile Memory Hierarchies**,"
in *Proc. the ACM Int'l Conf. Computing Frontiers (CF)*, May 2012.

Doe Hyun Yoon, Naveen Muralimanohar, Jichuan Chang, Parthasarathy Ranganathan, Norman P. Jouppi, and Mattan Erez,
"**FREE-p: A Practical End-to-End Nonvolatile Memory Protection Mechanism**,"
in *IEEE Micro, Special Issue: Micro's Top Picks from 2011 Computer Architecture Conferences (MICRO TOP PICKS)*, vol. 32, no. 3, pp. 79-87, May/Jun. 2012.

Min Kyu Jeong, Doe Hyun Yoon, Dam Sunwoo, Mike Sullivan, Ikhwan Lee, and Mattan Erez,
"**Balancing DRAM Locality and Parallelism in Shared Memory CMP Systems**,"
in *Proc. the Int'l Symp. High-Performance Computer Architecture (HPCA)*, Feb. 2012.

Doe Hyun Yoon, Min Kyu Jeong, and Mattan Erez,
"**Adaptive Granularity Memory Systems: A Tradeoff between Storage Efficiency and Throughput**,"
in *Proc. the 38th Ann. Int'l Symp. Computer Architecture (ISCA)*, Jun. 2011.

Doe Hyun Yoon and Mattan Erez,
" **Virtualized ECC: Flexible Reliability in Main Memory**,"
in *IEEE Micro, Special Issue: Micro's Top Picks from 2010 Computer Architecture Conferences (MICRO TOP PICKS)*, vol. 31, no. 1, pp. 11-19, Jan./Feb. 2011.

Doe Hyun Yoon, Naveen Muralimanohar, Jichuan Chang, Parthasarathy Ranganathan, Norman P. Jouppi, and Mattan Erez,
"**FREE-p: Protecting Non-Volatile Memory against both Hard and Soft Errors**,"
in *Proc. the Int'l Symp. High-Performance Computer Architecture Conference (HPCA)*, Feb. 2011.
One of the computer architecture papers of 2011 selected as Top Picks by IEEE Micro.

Doe Hyun Yoon and Mattan Erez,
"**Virtualized and Flexible ECC for Main Memory**,"
in *Proc. the Int'l. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Mar. 2010.
One of the computer architecture papers of 2010 selected as Top Picks by IEEE Micro.

Doe Hyun Yoon and Mattan Erez,
"**Flexible Cache Error Protection using an ECC FIFO**,"
in *Proc. the Int'l. Conf. High Performance Computing, Networking, Storage and Analysis (SC)*, Nov. 2009.

Doe Hyun Yoon and Mattan Erez,
"**Memory Mapped ECC: Low-Cost Error Protection for Last Level Caches**,"
in *Proc. the 36th Ann. Int'l. Symp. Computer Architecture (ISCA)*, Jun. 2009.

Hee-Suk Pang and Doe-Hyun Yoon,
"**Automatic Detection of Vibrato in Monophonic Music**,"
in *Elsevier Pattern Recognition*, vol. 38, no. 8, pp. 1135-1138, Aug. 2005.

Doe Hyun Yoon, Hee-Suk Pang, and Simon Ji,
"**Spiral Intra Macroblock Refresh with Motion Vector Restriction for Low Bit-Rate Video Telephony over a 3G Network**,"
in *IEEE Transactions on Consumer Electronics*, vol. 50, issue 4, pp. 1038-1043, Nov. 2004.

Hong-Sik Kim, Doe-Hyun Yoon, and S. Kang,
"**SRAM Transparent Testing Methodology using Dynamic Power Supply Current**,"
in *IEE Proc. Circuits Devices and Systems*, vol. 148, no. 4, pp. 217-222, Aug. 2001.

Doe-Hyun Yoon, Hong-Sik Kim, and Sungho Kang,
"**Dynamic Power Supply Current Testing for Open Defects in CMOS SRAMs**,"
in *ETRI Journal*, vol. 23, no. 2, pp. 77-84, Jun. 2001.

Doe Hyun Yoon, Hong Sik Kim, and Sungho Kang,
"**Dynamic Power Supply Current Test for CMOS SRAM**,"
in *Proc. the Int'l. Conf. VLSI and CAD (ICVC)*, pp. 399-402, Oct. 1999.

Workshops

"**VerMem: Versioned Memory using Multilevel-Cell NVRAM**,"
in *Non-Volatile Memories Workshop (NVMW)* (poster session), Mar. 2012.

"**FREE-p: Protecting Non-Volatile Memory against both Hard and Soft Errors**,"
in *Non-Volatile Memories Workshop (NVMW)*, Mar. 2011.

Invited Talk

"**BOOM: Enabling Mobile Memory Based Low-Power Server DIMMs**,"
at Yonsei University (May 2012) and Seoul National University (May 2012).

"**Virtualized ECC: Flexible Reliability in Memory Systems**,"
in *Architecture Highlights 2010 – IBM Architecture PIC Student Workshop*, Oct. 2010.

Tech Reports

Ikhwan Lee, Mehmet Basoglu, Michael Sullivan, Doe Hyun Yoon, Larry Kaplan, and Mattan Erez,
"**Survey of Error and Fault Detection Mechanisms**,"
Technical report, TR-LPH-2011-002, LPH Group, Dept. Electrical and Computer Engineering, The University of Texas at Austin, April, 2011.

Michael Sullivan, Doe Hyun Yoon, and Mattan Erez,
"**Containment Domains: A Full-System Approach to Computation Resiliency**,"
Technical report, TR-LPH-2011-001, LPH Group, Dept. Electrical and Computer Engineering, The University of Texas at Austin, Jannuary, 2011.

Granted US Patents

- Method for scalably encodign and decoding video signal, US 8,514,936
- Method for scalably encoding and decoding video signal, US 8,369,400
- Method for modeling coding information of a video signal to compress/decompress the information, US 8,331,453
- Method for modeling coding information of a video signal to compress/decompress the information, US 8,320,453
- Method for modeling coding information of video signal for compressing/decompressing coding information, US 8,306,117
- Method for modeling coding information of video signal for compressing/decompressing coding information, US 8,119,821
- Method for providing and using information about inter-layer prediction for video signal, US. 8,050,326
- Method for scalably encoding and decoding video signal, US 7,970,057
- Method for scalably encoding and decoding video signal, US 7,899,115
- Method for modeling coding information of a video signal for compressing/decompressing coding information, US 7,894,523
- Method for scalably encoding and decoding video signal, US 7,864,849
- Method for scalably encoding and decoding video signal, US 7,864,841
- Method of encoding and decoding video signals, US 7,813,428
- Method for scalably encoding and decoding video signal, US 7,787,540
- Method and apparatus for encoding/decoding video signal using reference pictures, US 7,746,933
- Method and apparatus for decoding video signal using reference pictures, US 7,688,897
- Method for scalably encoding and decoding video signal, US 7,627,034
- Method and apparatus for decoding video signal using reference pictures, US 7,593,467
- Method and apparatus for encoding/decoding video signal using reference pictures, US 7,586,985

Professional Activities

Program committee member: IPDPS 2012, SBAC-PAD 2013
Review committee member: SELSE 2013

References

Available upon request