BOOM: Enabling Mobile Memory Based Low-Power Server DIMMs

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Server Memory

Capacity demand
In-memory database
Memcached

Memory power
215W for 256GB
Even larger than CPU power
BOOM [Buffered Output On Module]

Buffered DIMM
Wide slow data bus
Mobile memory

Much lower power
Only 58W for 256GB

No compromise in performance & reliability

75% Reduction
Mobile Memory for Servers
## Mobile Memory Advantages

**Designed for low power, comparable latency**

<table>
<thead>
<tr>
<th></th>
<th>LPDDR2 x16</th>
<th>DDR3 x4/x8</th>
<th>DDR3 x16</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>1.2V</td>
<td>1.5V</td>
<td>1.5V</td>
</tr>
<tr>
<td>$I_{DD2P}$</td>
<td>1.6mA</td>
<td>35mA</td>
<td>40mA</td>
</tr>
<tr>
<td>I/O</td>
<td>Untermintaed</td>
<td>Terminated</td>
<td>Terminated</td>
</tr>
<tr>
<td>tRCD</td>
<td>15ns</td>
<td>13.75ns</td>
<td>13.75ns</td>
</tr>
<tr>
<td>tCL</td>
<td>15ns</td>
<td>13.75ns</td>
<td>13.75ns</td>
</tr>
<tr>
<td>Burst length</td>
<td>Burst 4</td>
<td>Burst 8</td>
<td>Burst 8</td>
</tr>
</tbody>
</table>
Can we use mobile memory for servers?
(Server) Memory Requirements

High capacity

High performance – high BW

Low power

Low cost – Total Cost of Ownership (TCO)

High reliability/availability – chipkill-correct

These objectives are inter-twined among others

Mobile memory can reduce server power, but may adversely affect other objectives
Chipkill-correct

System continuously functions even at a DRAM chip failure
Single DRAM chip failure correction and double DRAM chip failure detection
At least 2 ECC DRAM chips per logical rank
Reed Solomon code combined with erasure technique

Easier to implement chipkill with narrow (x4) DRAM chips

2 x4 ECC chips per 16 x4 data chips
12.5% overhead

2 x8 ECC chips per 8 x8 data chips
25% overhead

2 x16 ECC chips per 4 x16 data chips
50% overhead
## Mobile Memory for Low-Power Server DIMMs

<table>
<thead>
<tr>
<th><strong>Capacity</strong></th>
<th><strong>Cost</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>2-8Gb LPDDR2 is already available</td>
<td>Increasing market volume drives cost low</td>
</tr>
<tr>
<td>Buffered DIMMs can help</td>
<td>Low operating power can improve TCO</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Bandwidth</strong></th>
<th><strong>Reliability</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8GHz LPDDR2 vs. 1.6GHz DDR3</td>
<td>Only x16 and x32 devices</td>
</tr>
<tr>
<td>1.6GHz LPDDR3 vs. 3.2GHz DDR4</td>
<td>Difficult to enable chipkill-correct</td>
</tr>
</tbody>
</table>
How to enable high BW and chipkill-correct with mobile memory?
BOOM Architecture
Baseline Load-Reduced DIMM (LR-DIMM)

On-module buffer completely isolates external bus from internal bus
Allow a larger number of DIMMs per channel at high channel frequency

External and internal buses have the same channel width and frequency
High channel bandwidth → High DRAM frequency
Baseline Load-Reduced DIMM (LR-DIMM)

BOOM

Slow DRAM chips

Wide slow bus

High BW
Re-organize DIMM
Commodity DRAM

Changes:
• Routing within DIMM
• Buffer chip
• ECC handling at the memory controller

N times wide internal bus
1/N DRAM frequency – Low power
Chipkill-correct for wide DRAM chips (e.g., x16)

The same external BW

N2 & N4 architectures – DRAM chips running at ½ or ¼ of the bus frequency
Baseline LR-DIMM with DDR3-1600

- 8 DDR3-1600 memory channels
- Capacity: 256GB
- Peak BW: 104GB/s
- 2 channel lock-step mode for chipkill-correct
- Only 4 logical channels (128-bit wide)

Normalized DRAM power

- Background
- RD/WR
- ACT/PRE
- Buffer

64-bit wide physical rank

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BOOM N2 with DDR3-800

1/2 DRAM frequency – reduce background power
Same BW, Same capacity

128-bit wide Internal bus
No lock-step mode, but support chipkill-correct
8 logical channels (64-bit wide)
BOOM N4 with LPDDR2-400

1/4 DRAM frequency
LPDDR2 further reduces background power
Still, Same BW, Same capacity

Internal 256-bit wide channel
No lock-step mode – 8 logical channels
Support chipkill-correct even for x16 LPDDR2 DRAM
Wide internal channel increases ACT/PRE power

Normalized DRAM power

- Background
- RD/WR
- ACT/PRE
- Buffer
**BOOM N4 + Sub-Ranking**

**Sub-ranking (or rank-subsetting)**
Access two 128-bit wide sub-ranks independently

- Reduce ACT/PRE power
- Increased complexity in scheduling
- Higher ECC overhead

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**Normalized DRAM power**

- **x4**
- **x8**
- **x16**

**Background**
**ACT/PRE**
**RD/WR**
**Buffer**

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**MC**

- **400MHz**
- **1600MHz**
DRAM Power reduction with BOOM

- Low-freq DRAM reduces background power
- LPDDR2 further reduces background power, but N4 arch increases ACT/PRE power
- Sub-ranking saves ACT/PRE power
- Buffer and I/O power is the next challenge

1. Baseline @ 1600
2. BOOM N2 @ 800
3. BOOM N4 @ 400
4. BOOM N4 @ 400 + sub-ranking

75% DRAM power saving w/ BOOM
Implications for Future Memory Systems
Current high-BW solutions: e.g., GDDR5
Trading off capacity and reliability

Current low-power solutions: e.g., LPDDR
Trading off BW and reliability
Current high-BW solutions: e.g., GDDR5
Trading off capacity and reliability

Current low-power solutions: e.g., LPDDR
Trading off BW and reliability

Baseline x4

Baseline x8

Normalized DRAM Power

Normalized Execution Time

Low Power

High Performance

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Current high-BW solutions: e.g., GDDR5
Trading off capacity and reliability

Current low-power solutions: e.g., LPDDR
Trading off BW and reliability

Baseline x4
Baseline x8
Current high-BW solutions: e.g., GDDR5
Trading off capacity and reliability

Baseline x4

Current low-power solutions: e.g., LPDDR
Trading off BW and reliability

BOOM: Compromise neither capacity nor reliability

Future Solutions:
DRAM focused on low power
BOOM enables high BW, reliability, capacity

Baseline x8
Conclusions

**BOOM enables MOBILE MEMORY for servers**
Wide slow internal bus
Commodity DRAM chips

**DRAM power reduction**
75% saving on average, across memory intensive applications
Much lower background power
Energy-proportional memory system

**No compromise in BW and reliability**
Same external bandwidth, Same capacity
Support chipkill-correct for wide DRAM chips

More details [ECC, access granularity, row-buffer size, etc] in the paper
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